

STM32MP13XXAE_1DDR3L

Schematics not complete, only for layout example

Table of contents

- Sheet 1: Project overview (this page)
- Sheet 2: Top
- Sheet 3: STM32 MPU I/Os
- Sheet 4: Power MPU
- Sheet 5: Power discret
- Sheet 6: DDR3L 16bits
- Sheet 7: NAND 8bits

U_STM32MP13XXAE_1DDR3L_TOP
STM32MP13XXAE_1DDR3L_TOPSchDoc



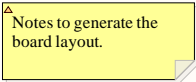
Note

Legend

General comment such as function title, configuration, ...

Text to be added to silkscreen.

Warning text.



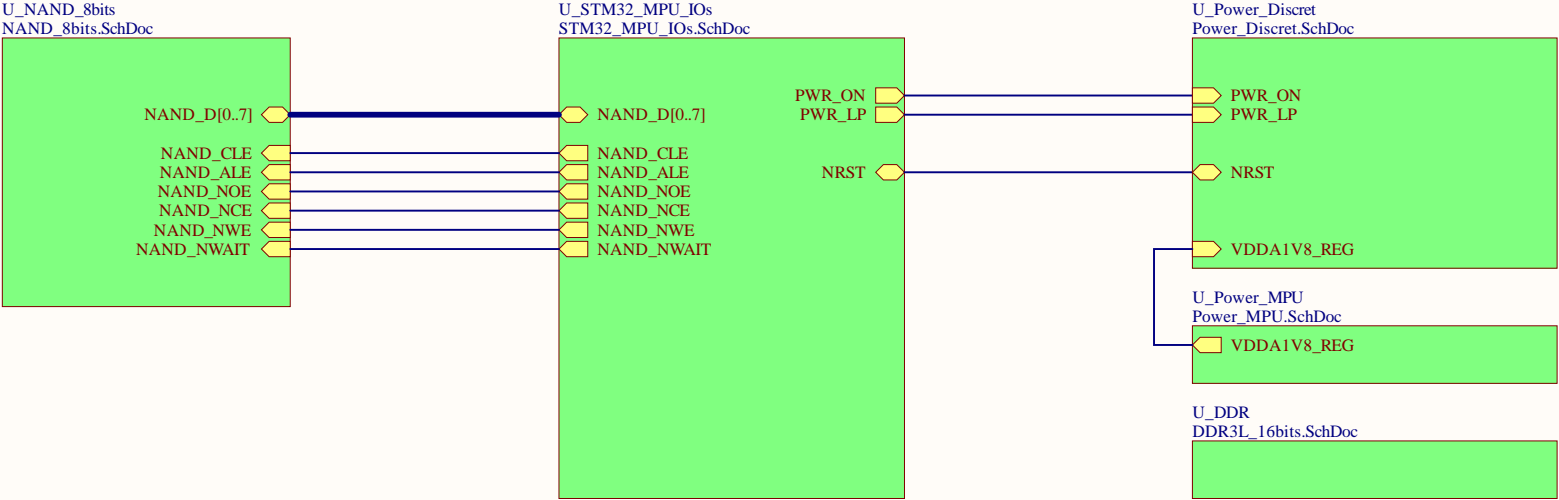
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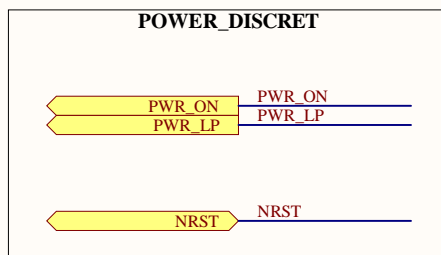
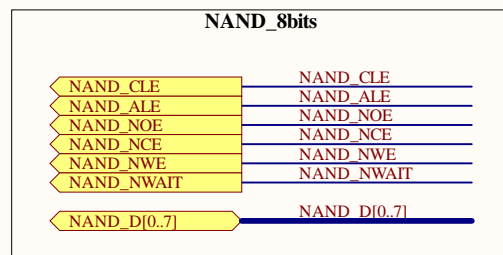
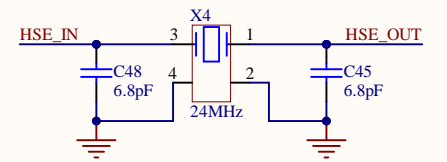
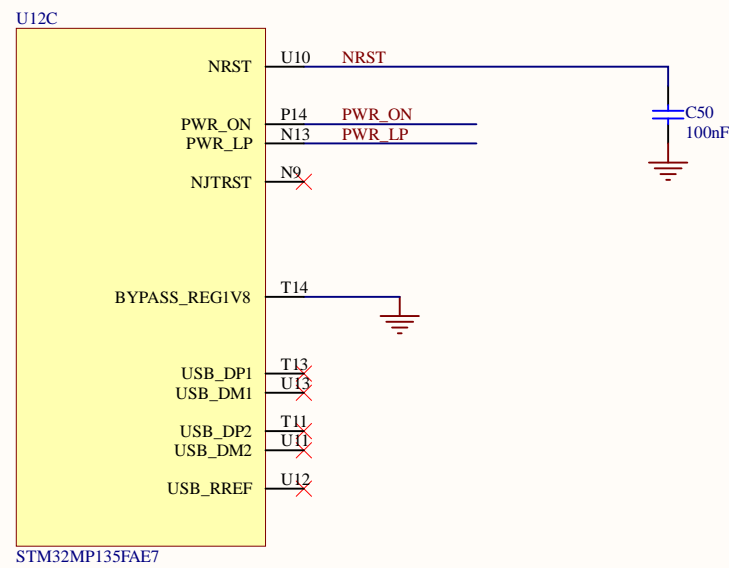
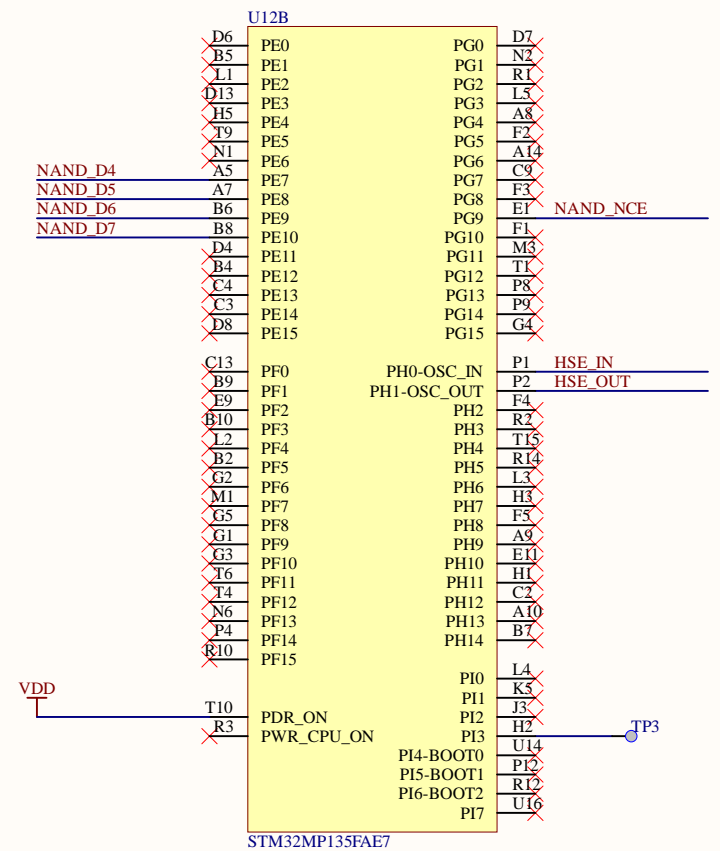
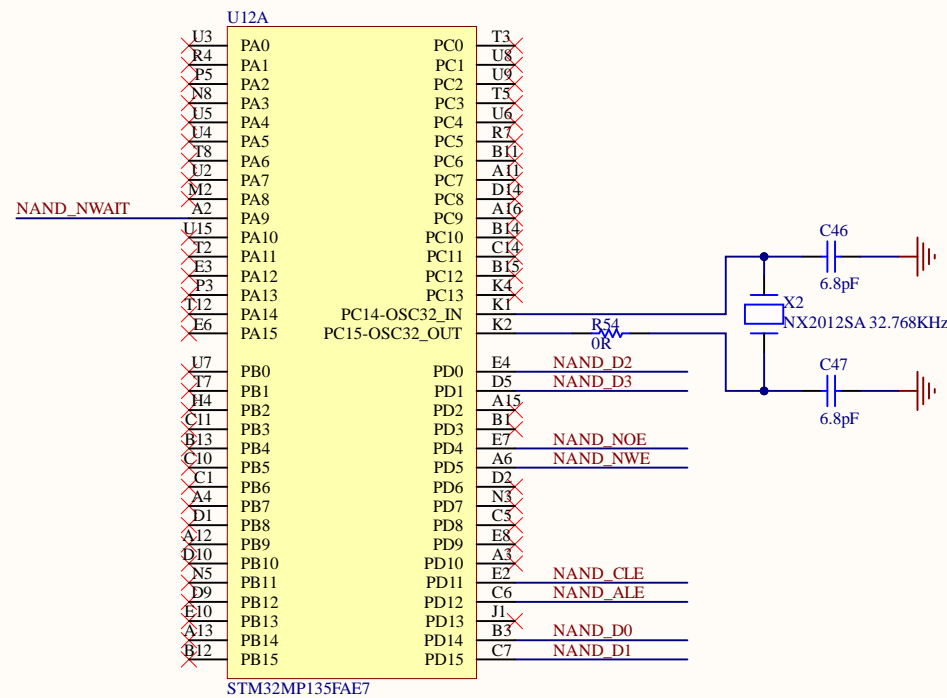
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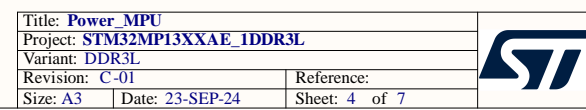
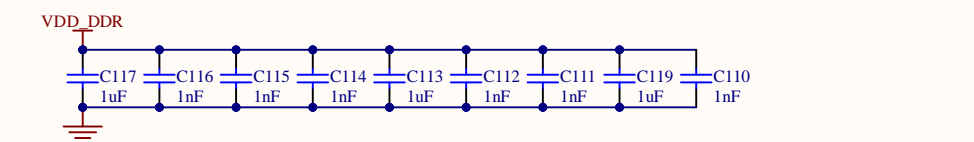
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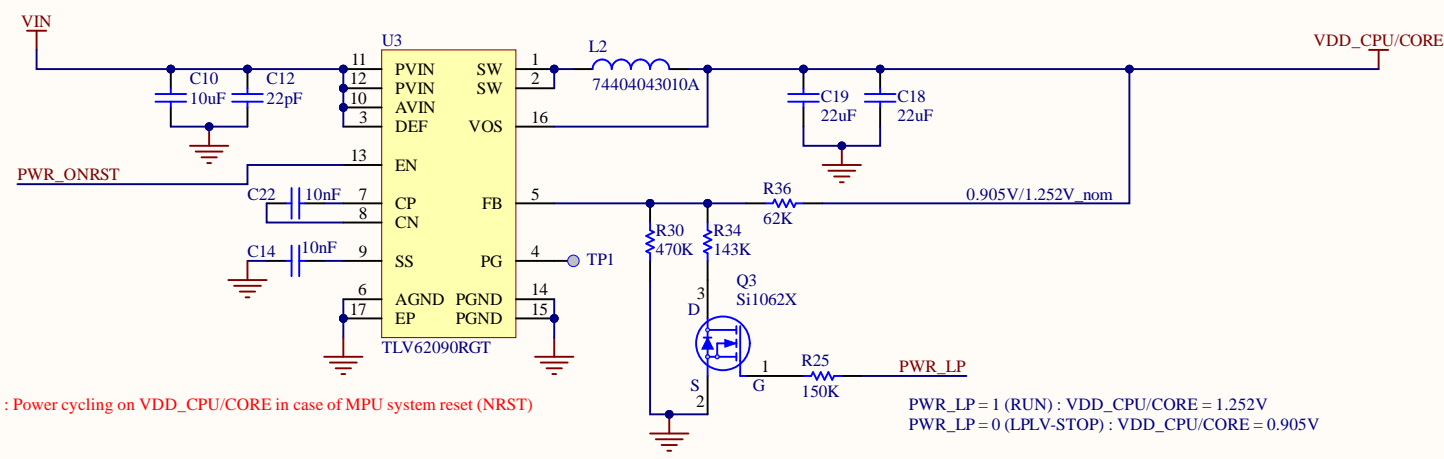
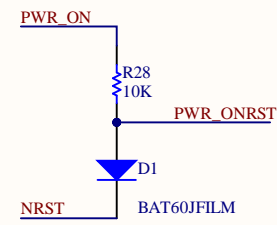
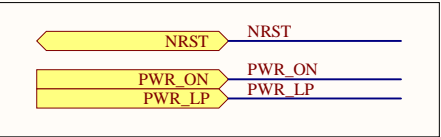
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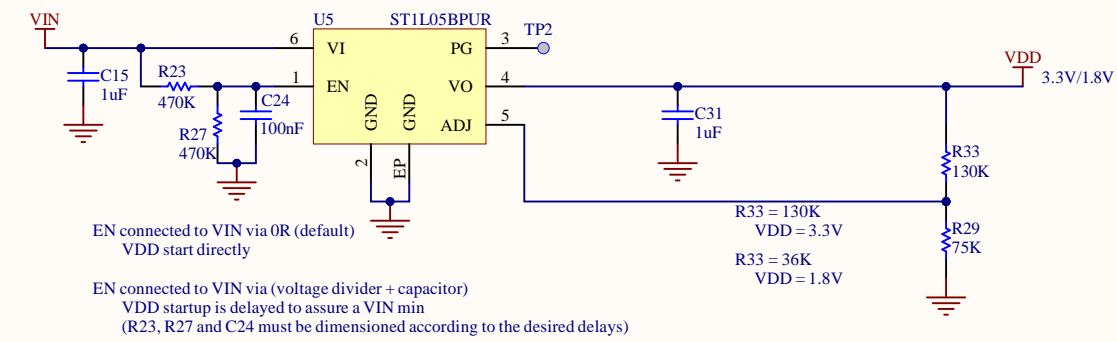




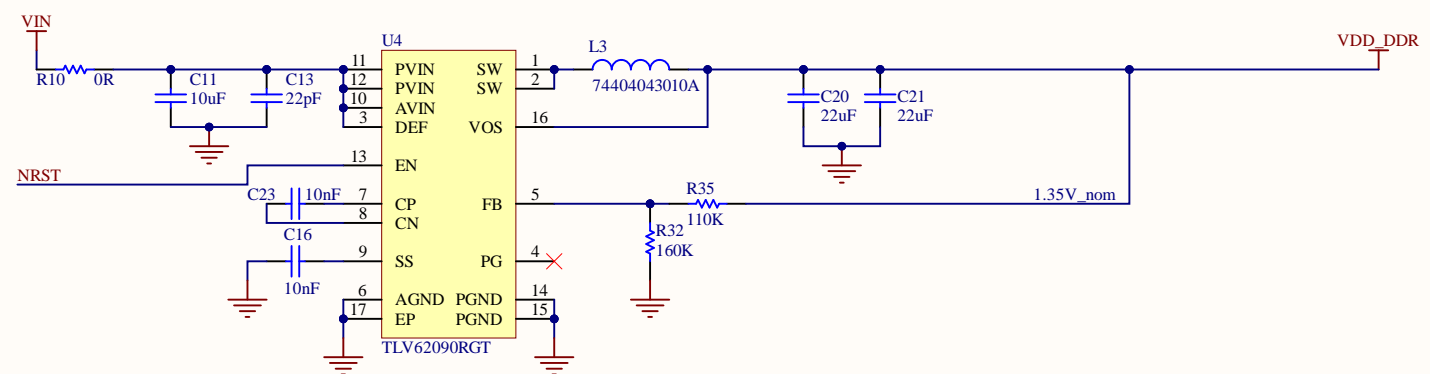




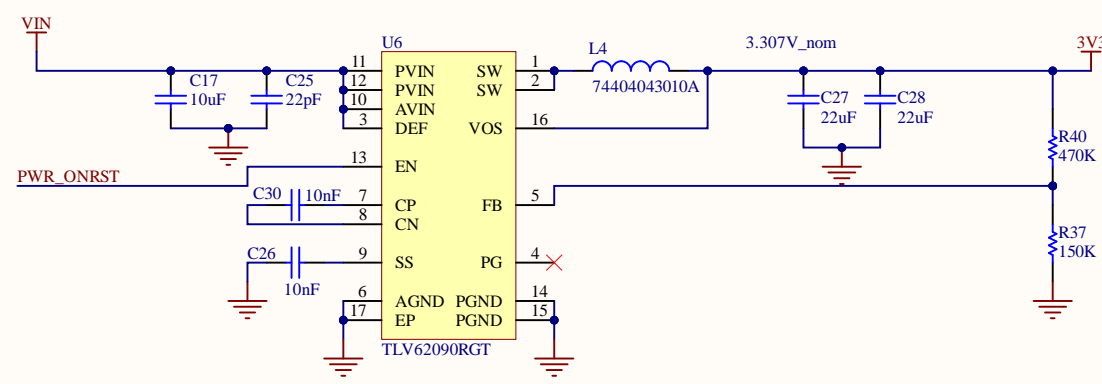
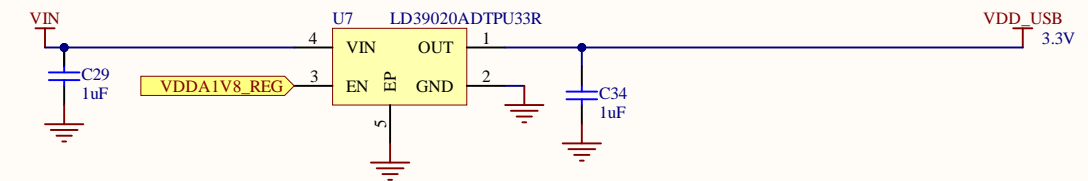
note: EN = PWR_ONRST : Power cycling on VDD_CPU/CORE in case of MPU system reset (NRST)
PWR_LP = 1 (RUN) : VDD_CPU/CORE = 1.252V
PWR_LP = 0 (LPLV-STOP) : VDD_CPU/CORE = 0.905V

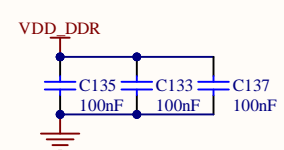
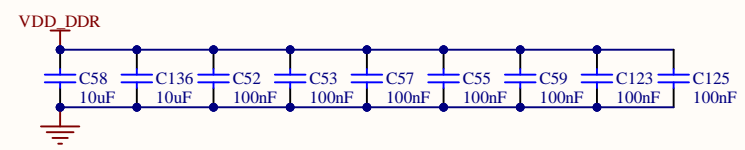
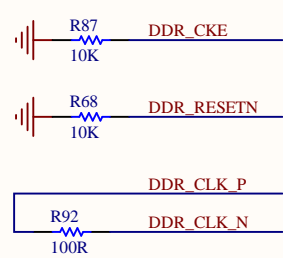
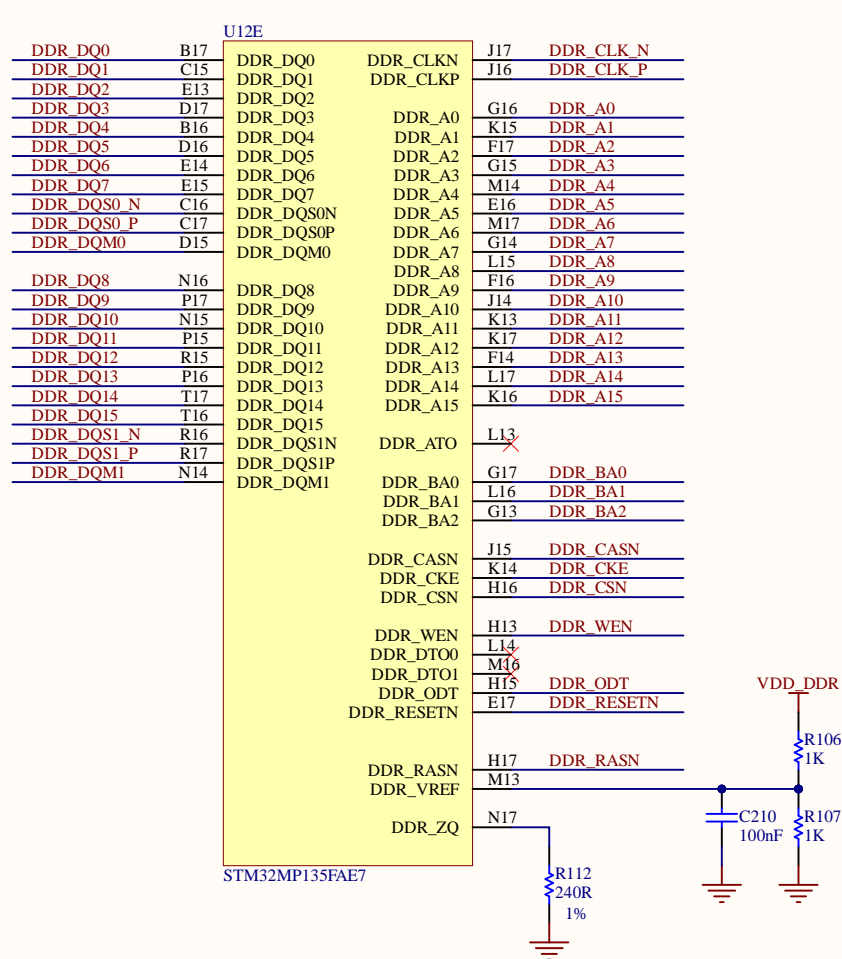


EN connected to VIN via 0R (default)
VDD start directly
EN connected to VIN via (voltage divider + capacitor)
VDD startup is delayed to assure a VIN min
(R23, R27 and C24 must be dimensioned according to the desired delays)



note: EN = NRST :DDR Powered ON in STANDBY mode (DDR retention mode)





To connect to VDD_DDR power plane

